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1 Generating highly-routable sparse crossbars for PLDs   100%
Guy Lemieux , Paul Leventis , David Lewis
Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000
> A method for evaluating and constructing sparse crossbars which are both area efficient and highly routable is presented. The evaluation method uses a network flow algorithm to accurately compute the percentage of random test vectors that can be routed. The construction method attempts to maximize the spread of the switch locations, such that any given subset of input wires can connect to as many output wires as possible. Based on Hall's Theorem, we argue that this increases the likelihood ...

2 The Transmogrifier-2: a 1 million gate rapid prototyping system   100%
David M. Lewis , David R. Galloway , Marcus van Ierssel , Jonathan Rose , Paul Chow
Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays February 1997

3 A hybrid complete-graph partial-crossbar routing architecture for multi- 100%
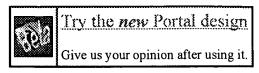FPGA systems
Mohammed A. S. Khalid , Jonathan Rose
Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays March 1998
> Multi-FPGA systems (MFSs) are used as custom computing machines, logic emulators

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Nagisa Ishiura , Shuzo Yajima
Proceedings of the conference on European design automation November 1992

2 Concepts and capabilities of a database computer\   89%
Jayanta Banerjee , David K. Hsiao , Richard I. Baum
ACM Transactions on Database Systems (TODS) December 1978
Volume 3 Issue 4
> The concepts and capabilities of a database computer (DBC) are given in this paper. The proposed design overcomes many of the traditional problems of database system software and is one of the first to describe a complete data-secure computer capable of handling large databases. This paper begins by characterizing the major problems facing today's database system designers. These problems are intrinsically related to the nature of conventional hardware and can only be solved by i ...

3 Poster session 1: A hybrid adiabatic content addressable memory for ultra low-power applications   88%
Aiyappan Natarajan , David Jasinski , Wayne Burleson , Russell Tessier
Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003
> This paper presents a hybrid adiabatic content addressable memory (CAM). The CAM uses an adiabatic switching technique to reduce the energy consumption in the match line while keeping the performance for the read/write operation. The adiabatic CAM is suitable for ultra low-power, low performance applications such as smart cards and